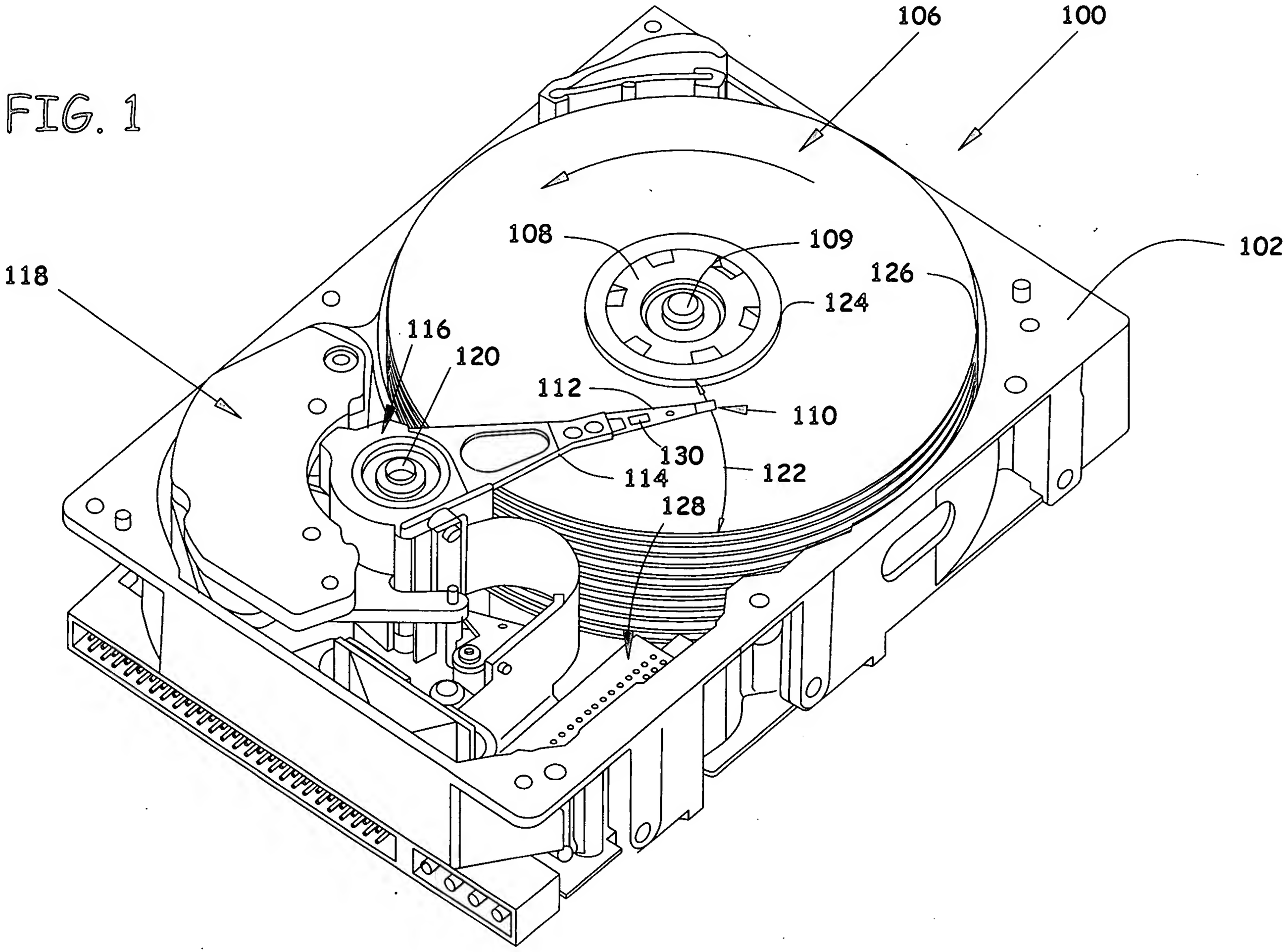
FIG. 1



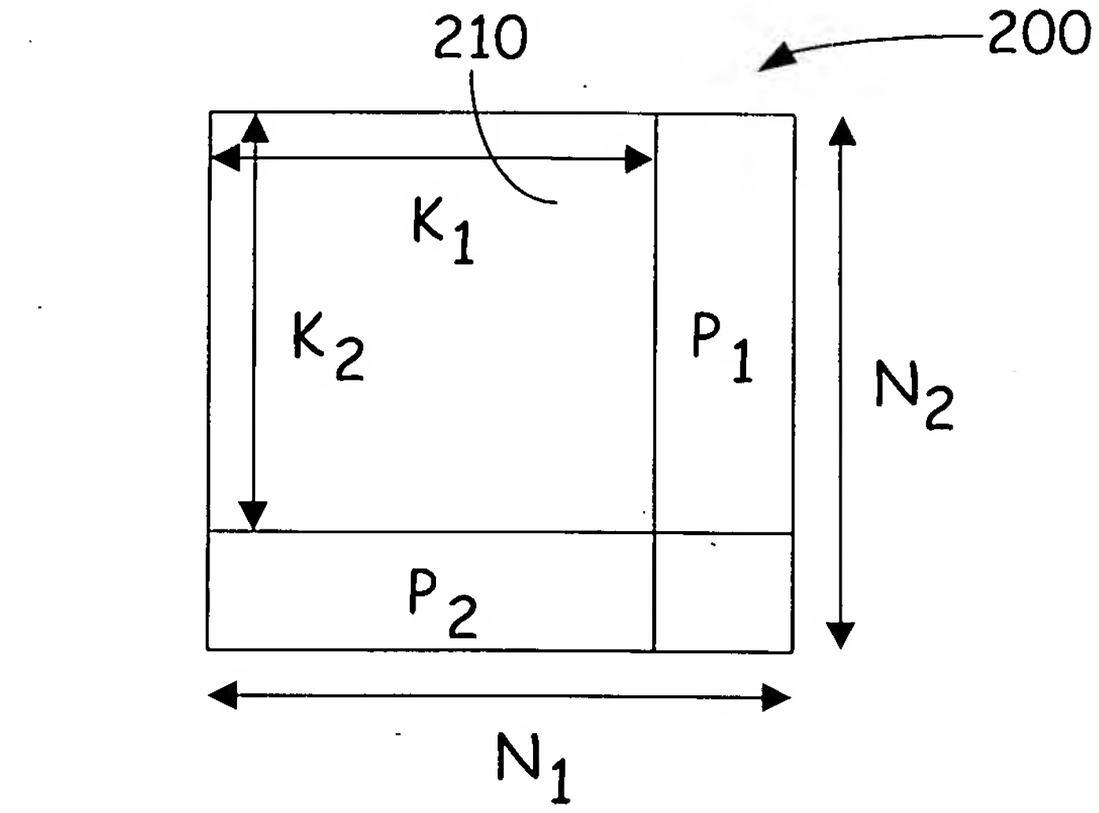


FIG. 2

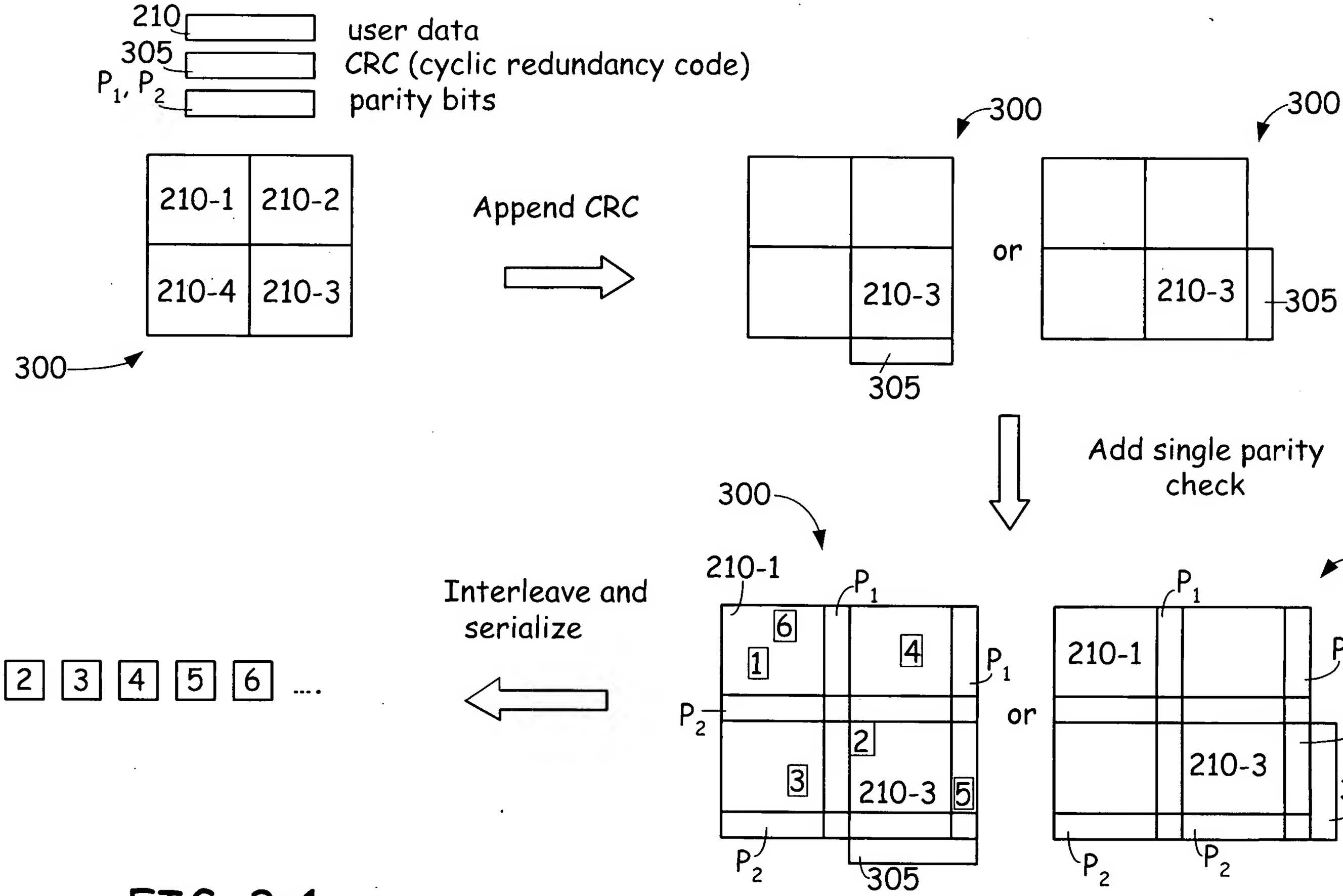

210
user data
305
CRC (cyclic redundancy code)
P1, P2
parity bits
210-1
210-2
210-4
210-3
300
Append CRC
300
210-3
305
or
300
210-3
305
Add single parity check
300
210-1
P1
6
1
4
P1
P2
2
3
210-3
5
P2
305
Interleave and serialize
1
2
3
4
5
6
....
300
210-1
P1
P1
P1
210-3
305
P2
P2
P2

FIG. 3-1

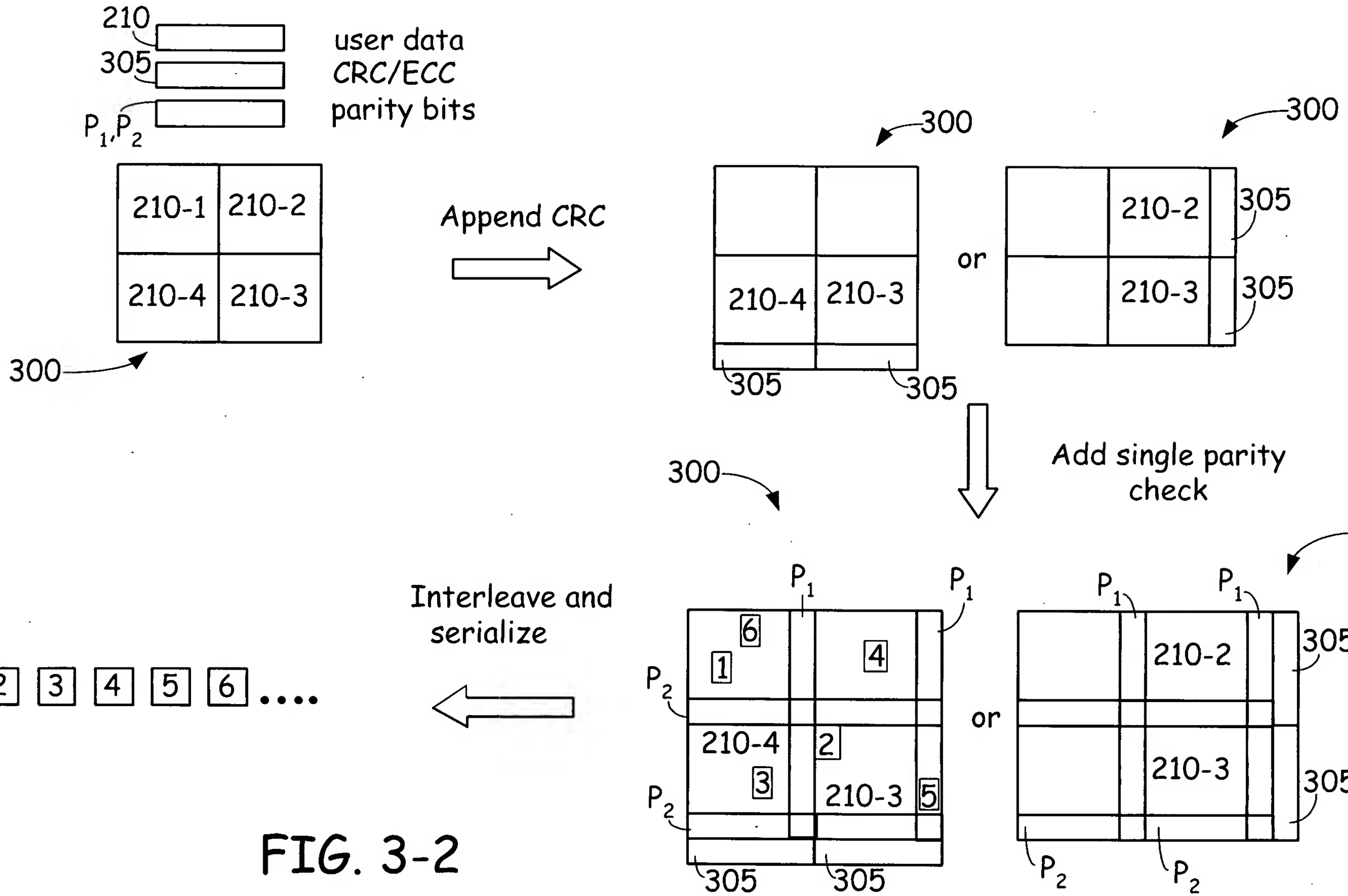

210
305
P1,P2
user data
CRC/ECC
parity bits
210-1
210-2
210-4
210-3
300
Append CRC
300
210-4
210-3
305
305
or
300
210-2
305
210-3
305
Add single parity check
300
Interleave and serialize
1
2
3
4
5
6
....
P1
P1
P2
6
1
4
210-4
2
3
210-3
5
P2
305
305
300
P1
P1
210-2
305
P2
210-3
305
P2
or

FIG. 3-2

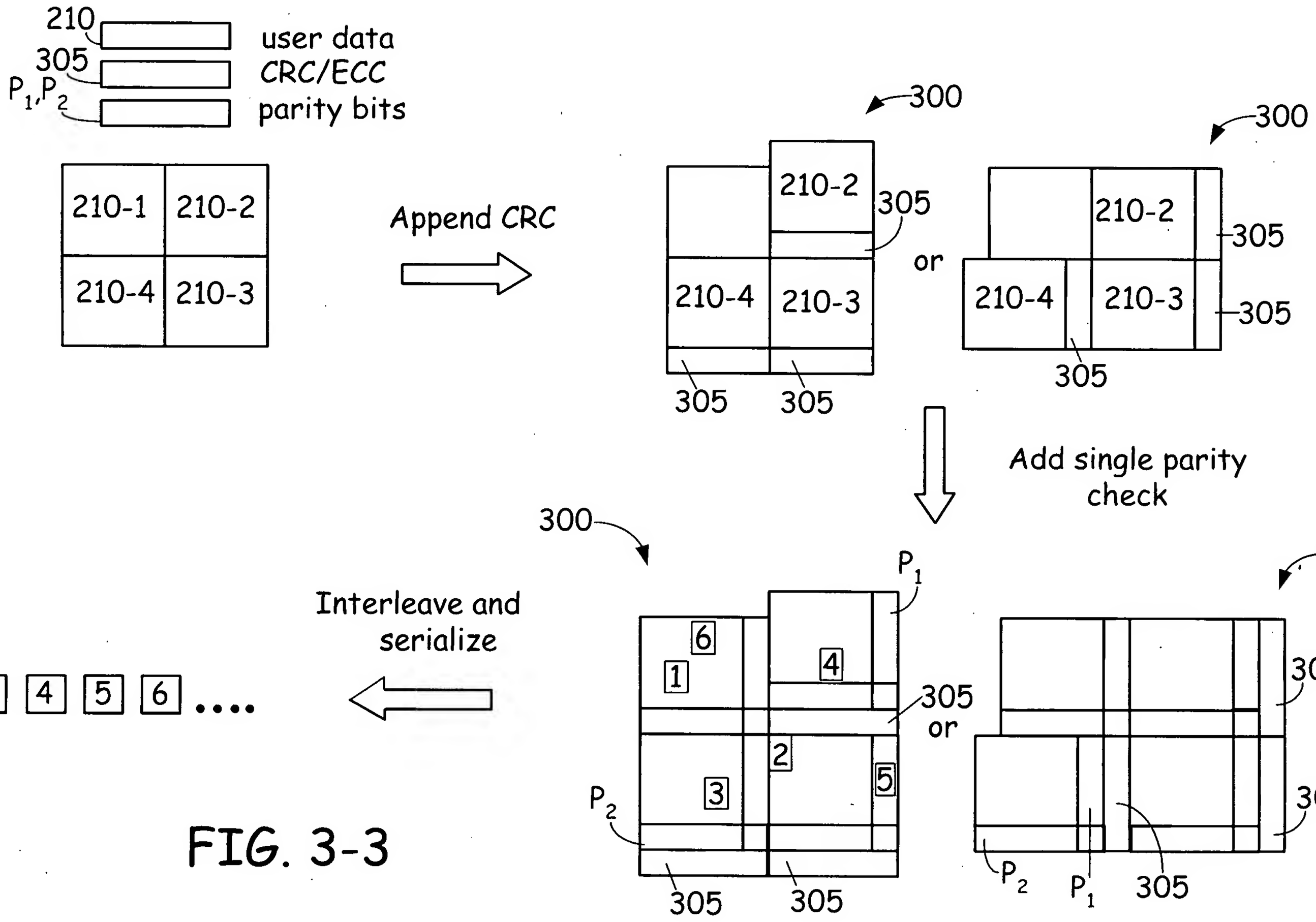

210
305
P_1, P_2
user data
CRC/ECC
parity bits
210-1
210-2
210-4
210-3
Append CRC
300
210-2
305
210-4
210-3
305
305
or
300
210-2
305
210-4
210-3
305
305
Add single parity check
300
P_1
6
1
4
305
or
2
3
5
P_2
305
305
300
305
305
P_2
P_1
305
Interleave and serialize
1 2 3 4 5 6 ....

FIG. 3-3

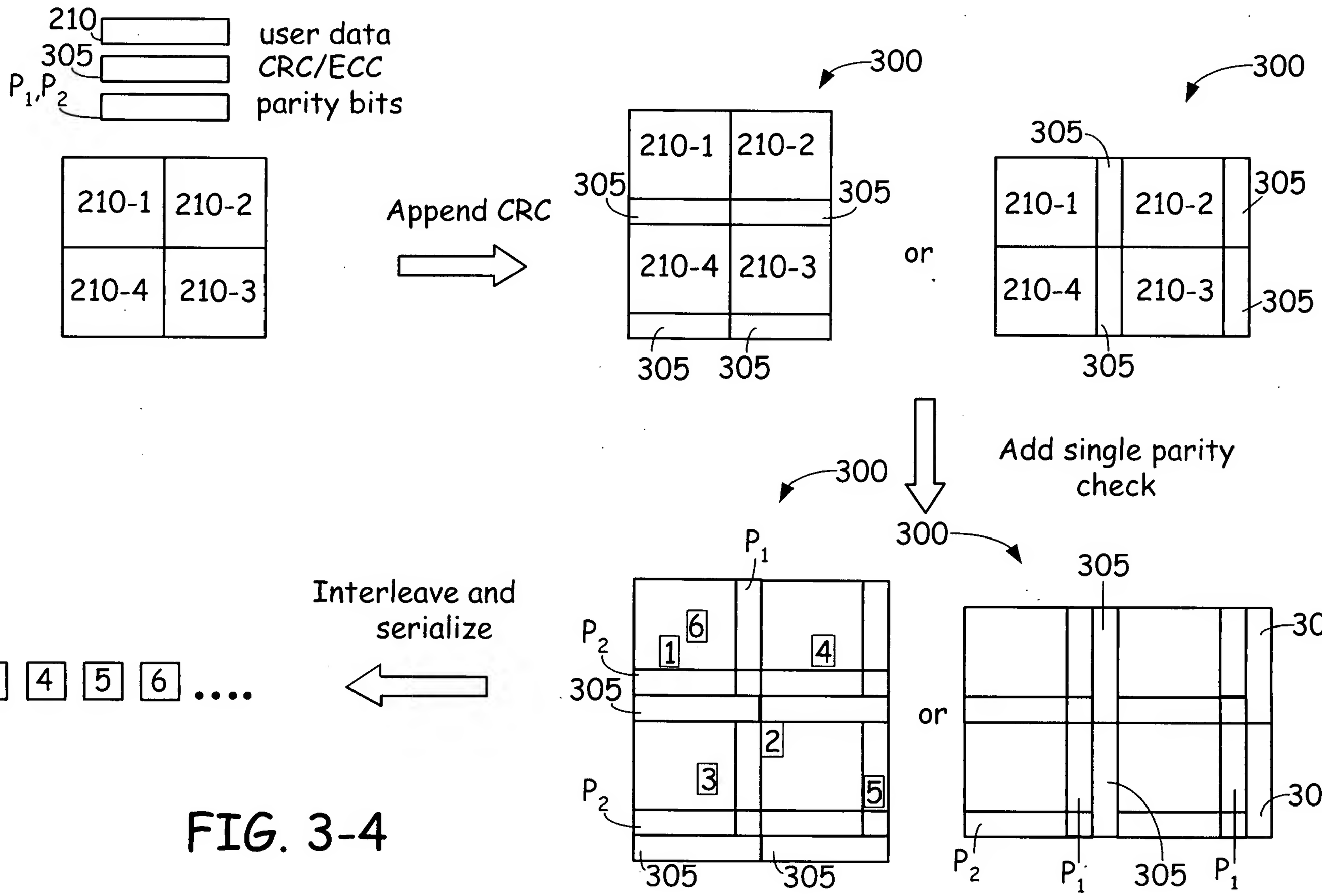

210
305
P_1, P_2
user data
CRC/ECC
parity bits
210-1
210-2
210-4
210-3
Append CRC
300
305
or
Add single parity check
Interleave and serialize
1 2 3 4 5 6 ....

FIG. 3-4

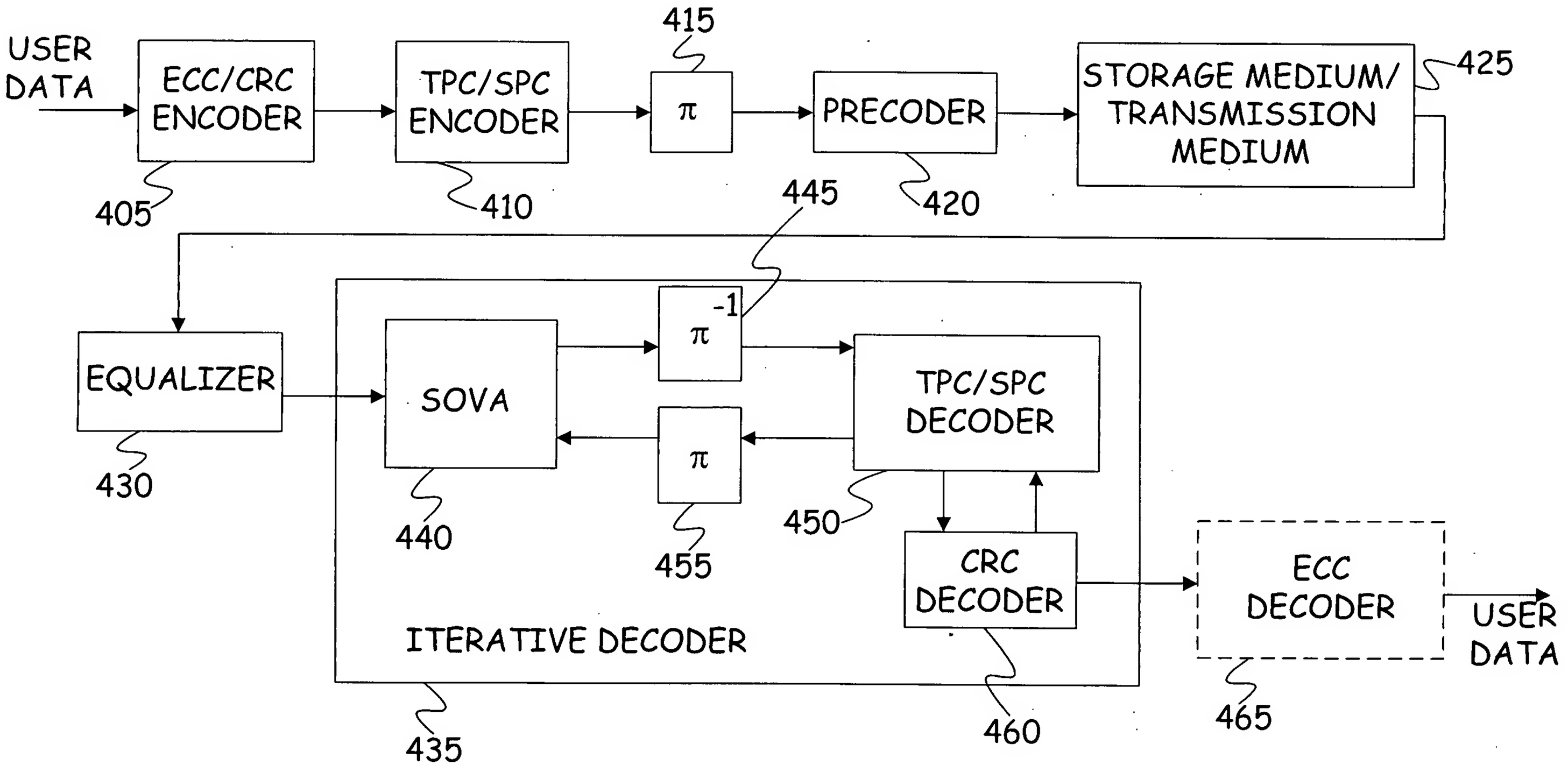

USER DATA
ECC/CRC ENCODER
TPC/SPC ENCODER
π
PRECODER
STORAGE MEDIUM/ TRANSMISSION MEDIUM
415
425
405
410
420
445
EQUALIZER
SOVA
π -1
π
TPC/SPC DECODER
CRC DECODER
ECC DECODER
USER DATA
ITERATIVE DECODER
430
440
455
450
435
460
465

FIG. 4

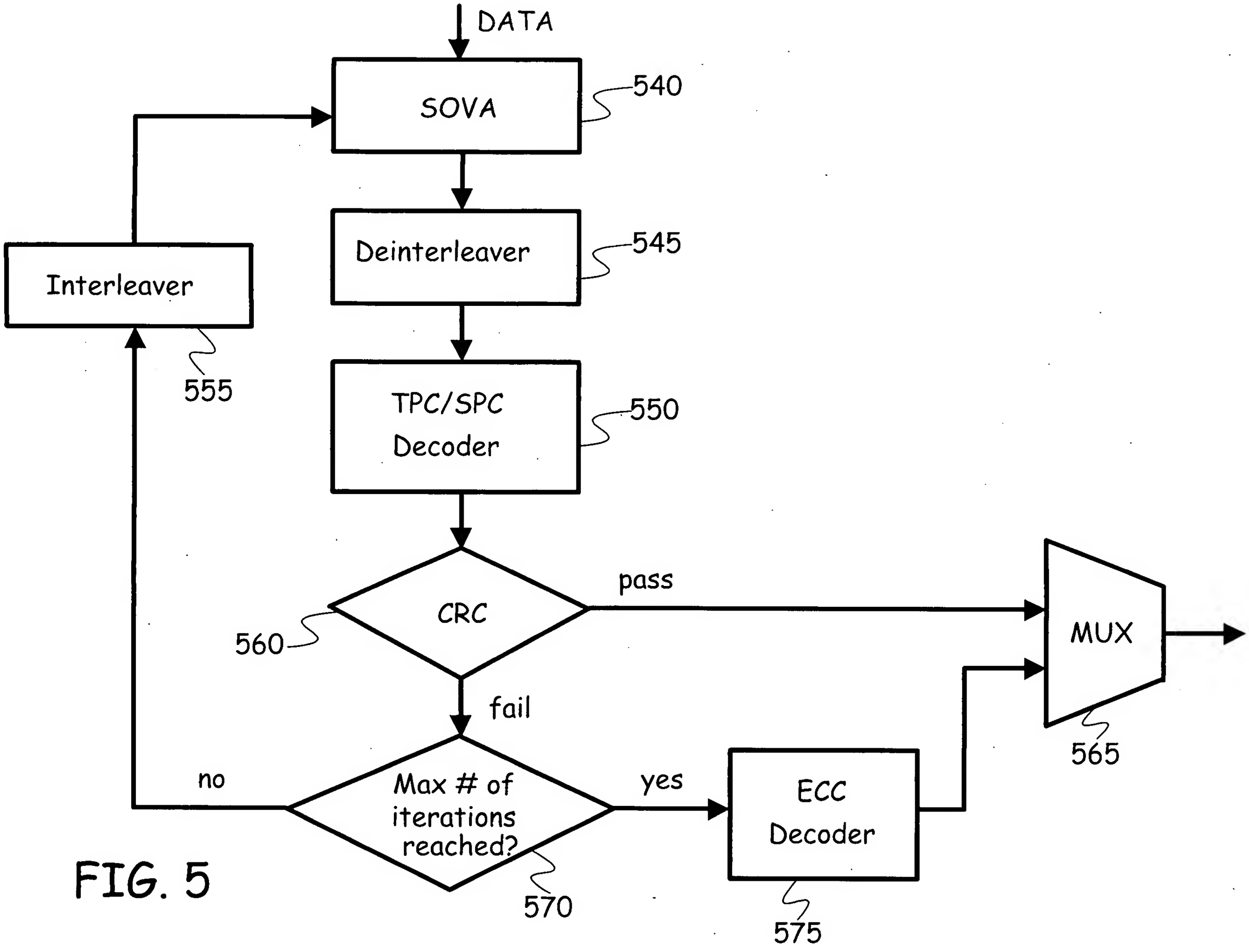

DATA
SOVA
540
Deinterleaver
545
Interleaver
555
TPC/SPC
Decoder
550
CRC
560
pass
fail
MUX
565
no
Max # of
iterations
reached?
570
yes
ECC
Decoder
575

FIG. 5

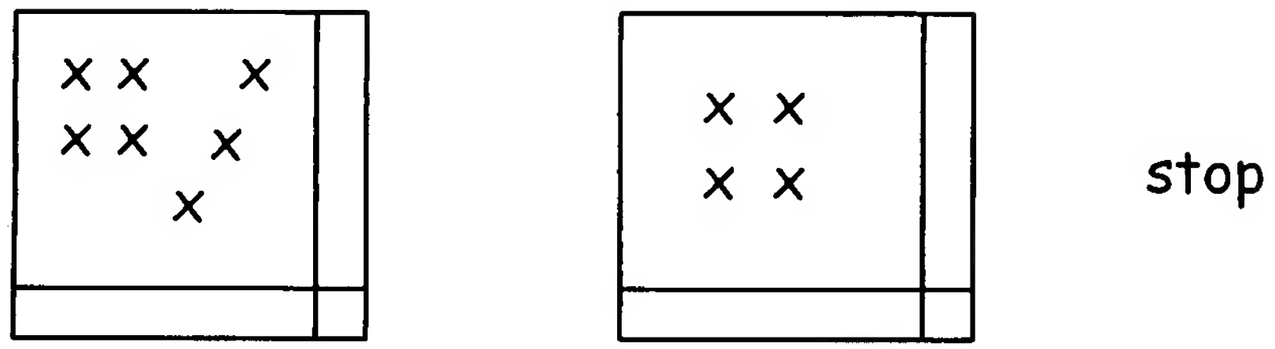

Iteration
#1
iteration
#2
stop
x = error bit

FIG. 6-1

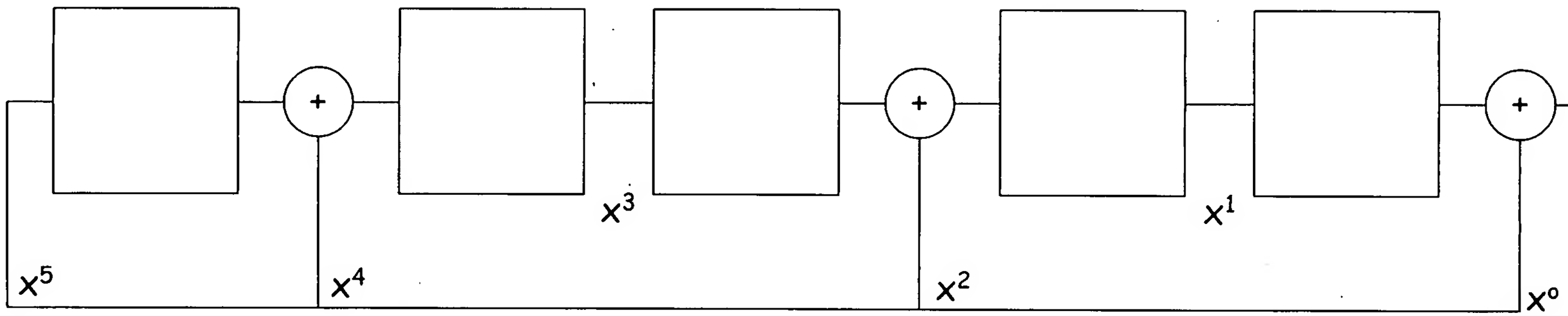
Iteration #1
iteration #2
.....
iteration #N
stop
x = error bit

FIG. 6-2

Input bits when creating CRC 1010000110100000

Input bits when creating CRC 1010000110101110

460



$P(x)=x^5+x^4+x^2+1$

FIG. 7

SNR = 6.4dB, 1600 codewords were simulated*

Termination Criterion	# of Error Events	# of wrong bits in those error events
Parity check Equation	44	4 10 4 14 6 2 4 4 4 1 8 4 4 6 8 4 1 4 4 4 6 12 2 4 2 4 4 4 4 2 10 3 4 4 4 4 4 6 4 4 8 4 4 1 4
CRC	5	1, 1, 2, 3, 1

*** SOVA/TPCSPC system With fixed-point calculation.**

FIG. 8

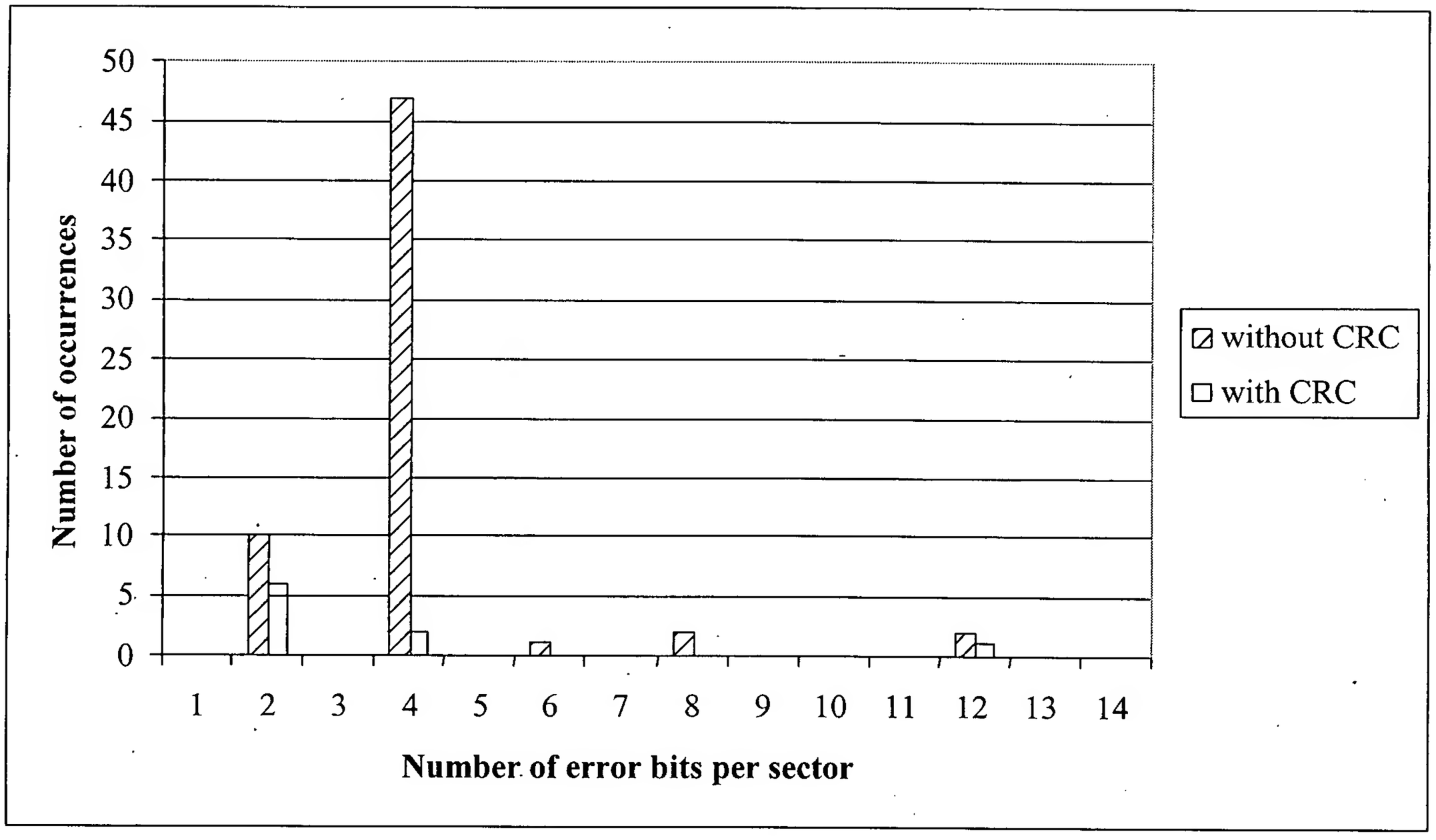

50
45
40
35
30
25
20
15
10
5
0
Number of occurrences
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Number of error bits per sector
without CRC
with CRC

FIG. 9